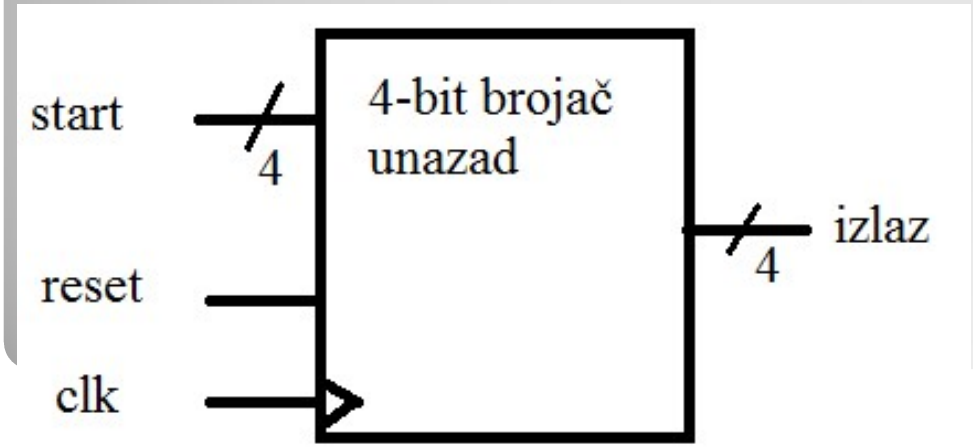
ZADATAK:

Napisati entitet i arhitekturu četvorobitnog brojača unazad, kod koga se posle svake rastuće ivice taktnog signala, stanje brojača smanjuje za 2 (binarno „10“). Brojač ima asinhroni **reset** kojim se izlaz postavlja u početno stanje kole se dovodi na **start** ulaznu magistralu.



VHDL modul

```
14  --
15  -- Revision:
16  -- Revision 0.01 - File Created
17  -- Additional Comments:
18  --
19  ----------------------------------------------------------------------------------
20  library IEEE;
21  use IEEE.STD_LOGIC_1164.ALL;
22  use IEEE.numeric_std.all;
23
24  entity BrojacUnazad is
25      Port ( clk : in  STD_LOGIC;
26             start : in  STD_LOGIC_VECTOR (3 downto 0);
27             rst : in  STD_LOGIC;
28             izlaz : out  STD_LOGIC_VECTOR (3 downto 0));
29  end BrojacUnazad;
30
31  architecture Behavioral of BrojacUnazad is
32  signal LokalniBrojac: unsigned (3 downto 0):=unsigned(start);
33  begin
34  Oduzmi4: process(clk,rst,start)
35  begin
36  if rst='1' then LokalniBrojac<=unsigned(start);
37  elsif (clk'event and clk='1') then LokalniBrojac<=LokalniBrojac - "10";
38  end if;
39  end process Oduzmi4;
40  izlaz<=std_logic_vector(LokalniBrojac);
41  end Behavioral;
42
43
```

```
28  LIBRARY ieee;
29  USE ieee.std_logic_1164.ALL;
30
31  -- Uncomment the following library declaration if using
32  -- arithmetic functions with Signed or Unsigned values
33  --USE ieee.numeric_std.ALL;
34
35  ENTITY BrojacUnazadTB IS
36  END BrojacUnazadTB;
37
38  ARCHITECTURE behavior OF BrojacUnazadTB IS
39
40      -- Component Declaration for the Unit Under Test (UUT)
41
42      COMPONENT BrojacUnazad
43      PORT(
44           clk : IN  std_logic;
45           start : IN  std_logic_vector(3 downto 0);
46           rst : IN  std_logic;
47           izlaz : OUT  std_logic_vector(3 downto 0)
48          );
49      END COMPONENT;
50
51
52     --Inputs
53     signal clk : std_logic := '0';
54     signal start : std_logic_vector(3 downto 0) := (others => '0');
55     signal rst : std_logic := '0';
56
```

```
57    --Outputs
58    signal izlaz : std_logic_vector(3 downto 0);
59
60    -- Clock period definitions
61    constant clk_period : time := 20 ns;
62
63  BEGIN
64
65    -- Instantiate the Unit Under Test (UUT)
66    uut: BrojacUnazad PORT MAP (
67           clk => clk,
68           start => start,
69           rst => rst,
70           izlaz => izlaz
71         );
72
73    -- Clock process definitions
74    clk_process :process
75    begin
76       clk <= '0';
77       wait for clk_period/2;
78       clk <= '1';
79       wait for clk_period/2;
80    end process;
81
82
83   start<="1111";
84   rst<='0','1' after 10ns,'0' after 30ns,'1' after 200ns,'0' after 210ns;
85  END;
86
```